1. A method of forming a damascene opening in the fabrication of an integrated circuit device comprising:

providing a region to be contacted in or on a substrate;

depositing a liner layer overlying said region to be contacted;

depositing a dielectric layer overlying said liner layer;

first etching said damascene opening through said dielectric layer to said liner layer overlying said region to be contacted wherein said first etching comprises a high F/C ratio etch chemistry, high power, and low pressure; and

second etching said liner layer within said damascene opening to expose said region to be contacted wherein said second etching comprises a high F/C ratio etch chemistry, low power, and low pressure to complete formation of said damascene opening in said fabrication of said integrated circuit device.

2. The method according to Claim 1 wherein said region to be contacted is selected from the group containing: a gate electrode, a source region, a drain regions, and a metal line.

3. The method according to Claim 1 wherein said liner layer is selected from the group containing silicon nitride and silicon carbide and has a thickness of between about 300 and 700 Angstroms.

4. The method according to Claim 1 wherein said dielectric layer has a dielectric constant of less than 2.5.

5. The method according to Claim 1 wherein said dielectric layer is selected from the group containing: Black Diamond and organic dielectric materials and has a thickness of between about 6000 and 10,000 Angstroms.

6. The method according to Claim 1 wherein said high F/C ratio etch chemistry of said first etching comprises CF_4 gas flowed at 0 to 150 sccm, O_2 gas flowed at 2 to 20 sccm, and Ar gas flowed at 0 to 300 sccm.

7. The method according to Claim 1 wherein said high power of said first etching comprises 700 to 1000 watts.

8. The method according to Claim 1 wherein said low pressure of said first etching comprises between about 80 and 150 mTorr.

9. The method according to Claim 1 wherein said high F/C ratio etch chemistry of said second etching comprises CF_4 gas flowed at 0 to 80 sccm and O_2 gas flowed at 0 to 50 sccm.

10. The method according to Claim 1 wherein said high F/C ratio etch chemistry of said second etching comprises CHF_3 gas flowed at 0 to 80 sccm and O_2 gas flowed at 0 to 50 sccm.

11. The method according to Claim 1 wherein said low power of said second etching comprises 250 to 500 watts.

12. The method according to Claim 1 wherein said low pressure of said second etching comprises between about 30 and 70 mTorr.

13. The method according to Claim 1 further comprising:

depositing a barrier metal layer within said damascene opening;

depositing a metal layer overlying said barrier metal layer; and

polishing down said metal layer to leave said metal layer only within said damascene opening.

14. The method according to Claim 13 wherein said metal layer is selected from the group containing copper and aluminum-copper alloys.

15. A method of forming a damascene opening in the fabrication of an integrated circuit device comprising:

providing a region to be contacted in or on a substrate;

depositing a liner layer overlying said region to be contacted;

depositing a dielectric layer overlying said liner layer wherein said dielectric layer has a dielectric constant of less than 2.5;

first etching said damascene opening through said dielectric layer to said liner layer overlying said region to be contacted wherein said first etching comprises a high F/C ratio etch chemistry, power of between 700 and 1000 watts, and pressure of between 20 and 150 mTorr; and

second etching said liner layer within said damascene opening to expose said region to be contacted wherein said second etching comprises a high F/C ratio etch chemistry, power of between 250 and 500 watts, and pressure of between 30 and 70 mTorr to complete formation of said damascene opening in said fabrication

of said integrated circuit device.

16. The method according to Claim 15 wherein said region to be contacted is selected from the group containing: a gate electrode, a source region, a drain regions, and a metal line.

17. The method according to Claim 15 wherein said liner layer is selected from the group containing silicon nitride and silicon carbide and has a thickness of between about 300 and 700 Angstroms.

18. The method according to Claim 15 wherein said dielectric layer is selected from the group containing: Black Diamond and organic dielectric materials and has a thickness of between about 6000 and 10,000 Angstroms.

19. The method according to Claim 15 wherein said high F/C ratio etch chemistry of said first etching comprises CF_4 gas flowed at 0 to 150 sccm, O_2 gas flowed at 0 to 20 sccm, and Ar gas flowed at 0 to 300 sccm.

20. The method according to Claim 15 wherein said high F/C ratio etch chemistry of said second etching comprises CF_4 gas flowed at 0 to 80 sccm and O_2 gas

flowed at 0 to 50 sccm.

21. The method according to Claim 15 wherein said high F/C ratio etch chemistry of said second etching comprises CHF_3 gas flowed at 0 to 80 sccm and O_2 gas flowed at 0 to 50 sccm.

22. The method according to Claim 15 further comprising:

depositing a barrier metal layer within said damascene opening;

depositing a metal layer overlying said barrier metal layer; and

polishing down said metal layer to leave said metal layer only within said damascene opening.

23. The method according to Claim 22 wherein said metal layer is selected from the group containing copper and aluminum-copper alloys.

24. A method of copper metallization in the fabrication of an integrated circuit device comprising:

providing a region to be contacted in or on a substrate;

depositing a liner layer overlying said region to be contacted;

depositing a dielectric layer overlying said liner layer wherein said dielectric layer has a dielectric constant of less than 2.5;

first etching said damascene opening through said dielectric layer to said liner layer overlying said region to be contacted wherein said first etching comprises a high F/C ratio etch chemistry, power of between 700 and 1000 watts, and pressure of between 20 and 150 mTorr;

second etching said liner layer within said damascene opening to expose said region to be contacted wherein said second etching comprises a high F/C ratio etch chemistry, power of between 250 and 500 watts, and pressure of between 30 and 70 mTorr;

depositing a barrier metal layer within said damascene opening;

depositing a copper layer overlying said barrier metal layer; and

polishing down said copper layer and said barrier metal layer to leave said barrier metal layer and said copper layer only within said damascene opening to complete said copper metallization in said fabrication of said integrated circuit device.

25. The method according to Claim 24 wherein said region to be contacted is selected from the group containing: a gate electrode, a source region, a drain regions, and a metal line.

26. The method according to Claim 24 wherein said liner layer is selected from the group containing silicon nitride and silicon carbide and has a thickness of between about 300 and 700 Angstroms.

27. The method according to Claim 24 wherein said dielectric layer is selected from the group containing: Black Diamond and organic dielectric materials and has a thickness of between about 6000 and 10,000 Angstroms.

28. The method according to Claim 24 wherein said high F/C ratio etch chemistry of said first etching comprises CF_4 gas flowed at 0 to 150 sccm, O_2 gas flowed at 0 to 20 sccm, and Ar gas flowed at 0 to 300 sccm.

29. The method according to Claim 24 wherein said high F/C ratio etch chemistry of said second etching comprises CF_4 gas flowed at 0 to 80 sccm and O_2 gas flowed at 0 to 50 sccm.

30. The method according to Claim 24 wherein said high F/C ratio etch chemistry of said second etching comprises CHF_3 gas flowed at 0 to 80 sccm and O_2 gas flowed at 0 to 50 sccm.